REMARKS

Responsive to the Official Action mailed July 13, 2005, Applicant provides the following remarks. Reconsideration and allowance of the subject application are respectfully requested.

Applicant has amended claims 43, 49, and 56 to correct minor typographical errors. No new matter has been entered.

35 USC §102 Rejections of the Claims

Claim 41 – 44 and 47 - 49 were rejected under 35 USC §102(b) as being anticipated by Yang et al (U.S. Patent No. 6,404,175, hereinafter "Yang"). The Examiner argues that Yang discloses:

> "a DC-DC converter (figure 4), including a comparator (figure 2, item 208) and a first signal (figure 2, from item VREF) and an offset signal (figure 2, items output of item 212), pulse width modulation (figure 2, item PWM), the output voltage different than pre established value (column 3, line 55-65), a pair of switches (figure 2, item Q1 and Q2) and a periodic reference (column 3, line 60 – 65)." Official Action dated July 13, 2005, page 2-3, ¶ #2.

Applicant respectfully traverses this rejection. Applicant's claim 41 requires "a comparator configured to compare a first signal representative of an output voltage of said DC-DC converter with a periodic reference signal having a DC offset determined by a DC reference voltage source," (emphasis added.) For example, FIG. 1 of Applicant's specification illustrates a comparator 118 configured to compare a signal representative of an output voltage via feedback loop 124 with a periodic reference signal 126 having a DC offset determined by the DC voltage source 114.

Yang's FIG. 2 teaches elimination of a conventional sense resistor by utilizing "the inductive resistance, R_L 206, of the filter inductor winding 202." Column 3, lines 42 – 43. The voltage drop across the inductive resistance R_L 206 is "detectable by the differential amplifier 204 since the large Ldi/dt voltage across both the windings 200, 202 cancel one another." Column 3, lines 49 – 51. Yang then teaches the "differential amplifier 204 output is then used with conventional feedback control circuitry to adjust the conduction duty cycle of the phase." Column 3, lines 53 – 55.

The PWM comparator 208 of Yang's FIG. 2 receives an error signal from the error amplifier 212 of the feedback control circuitry and a conventional periodic saw-tooth waveform. For instance, Yang teaches "[t]he error voltage generated by the error amplifier 212 acts as one input to a pulse width modulator (PWM) comparator 208 whose other input is a periodic saw-tooth waveform." (emphasis added.) Column 3, lines 59 – 62.

In contrast, claim 41 requires "a comparator configured to compare first signal representative of an output voltage of said DC-DC converter with a periodic reference signal having a DC offset determined by a DC reference voltage source". Yang simply does not teach, disclose or suggest this limitation. Accordingly, Applicant respectfully submits Yang cannot anticipate claim 41, and thus, claim 41 is allowable.

Claims 42 - 46 depend, directly or indirectly, from claim 41. Therefore, Applicant respectfully submits claims 42 - 46 are also allowable by virtue of their dependency from claim 41 in addition to their own patentable limitations.

Claim 47 is directed to a DC to DC converter "a means for comparing a first signal representative of an output voltage of said DC-DC converter with a periodic reference signal

having a DC offset determined by a DC reference voltage source and providing an output signal that drives said output voltage of said DC-DC converter towards a pre-established value." (emphasis added.) For similar reasons adduced above regarding independent claim 41, Applicant respectfully submits claim 47 is also allowable. Claims 48 - 49 depend, directly or indirectly, from claim 47. Therefore, Applicant respectfully submits claims 48 - 49 are also allowable by virtue of their dependency from claim 47 in addition to their own patentable limitations.

The Examiner also rejected claim 50 under 35 USC §102(b) as being anticipated by Barkaro (US Pat. No. 5,949,224). Applicant respectfully traverses this rejection.

Barkaro is directed to a buck boost switching regulator. FIG. 1 of Barkaro teaches a comparator 4 to provide a control signal to the transistor 1 (buck switch) and a comparator 5 to provide a control signal to transistor 2 (boost switch). Each comparator 4 and 5 receives a ramp signal from the ramp generator 6. Barkaro teaches the ramp generator 6 is "adapted to generate a recurrent ramp signal, while the other input of the comparator 4 is connected to the output of the amplifier 7." Column 2, line 10 - 12.

Claim 50 is directed to a method of controlling an output voltage of a DC to DC converter comprising "comparing a first signal representative of an output voltage of said DC-DC converter with a periodic reference signal having a DC offset determined by a DC reference voltage source." (emphasis added.) There is no teaching, suggestion, or disclosure in Barkaro that the ramp signal provided by the ramp generator 6 has "a DC offset determined by a DC reference voltage source" as required by claim 50.

Accordingly, Applicant respectfully submits claim 50 is allowable. Claims 51 depends from claim 50. Therefore, Applicant respectfully submits claim 51 is also allowable by virtue of its dependency from claim 50 in addition to its own patentable limitations.

The Examiner also rejected claims 52 – 59 under 35 USC §102(e) as being anticipated by Redl et al (US Pat. No. 6,229,292, hereinafter "Redl"). The Examiner argues Redl teaches a comparator (figure 1, item 22 and 28). Applicant respectfully traverses this rejection.

Redl is generally directed to a circuit and method to "enable a voltage regulator to employ the smallest possible output capacitor that allows the regulator's output voltage to be maintained within specified boundaries for large bidirectional step changes in load current." (Abstract of Redl) FIG. 1 of Redl discloses a switching regulator 10 that includes comparators 28 and 22. Comparator 28 "receives a reference voltage V_{ref} at one input and a voltage representative of the output voltage V_{out} at a second input, and produces an error voltage that varies with the difference between V_{out} and the desired output voltage." Column 2, lines 17 – 20. This comparator 28 is not configured "to compare a first signal representative of an output voltage with a periodic reference signal having a DC offset determined by a DC reference voltage source" as required by claim 52.

The comparator 22 of the switching regulator 10 "compares a sawtooth clock signal received from a clock circuit 24 and an error voltage received from an error signal generating circuit 26." Column 2, lines 13 – 15. The error voltage received from the error generating circuit 26 is provided by the other comparator 28. The sawtooth clock signal does not have "a DC offset determined by a DC reference voltage source" as required by claim 52. In summary, neither comparator 28 or comparator 22 nor any other comparator of Redl are configured "to

compare a first signal representative of an output voltage with a periodic reference signal having a DC offset determined by a DC reference voltage source" as required by claim 52.

Accordingly, Applicant respectfully submits claim 52 is allowable. Claims 53 – 59 depend, directly or indirectly, from claim 52. Therefore, Applicant respectfully submits claims 53 – 59 are also allowable by virtue of their dependency from claim 52 in addition to their own patentable limitations

Double Patenting

The Examiner also rejected claims 41 – 59 under the judicially created doctrine of obviousness-type double patenting. Enclosed is a Terminal Disclaimer to obviate the double patenting rejection over claims 13 - 23 of U.S. Patent No. 6,459,602. Therefore, no further discussion of the Double Patenting rejection is believed necessary. Also enclosed is a credit card authorization form authorizing a charge in the amount of $130.00 to cover the Terminal Disclaimer fee. In the event there are any additional fees due, please charge them to our Deposit Account No. 50-2121.

In light of the foregoing, it is believed that all of the presently pending claims 41 – 59 are in a condition for allowance. Allowance of the application is respectfully requested. In the event the Examiner deems personal contact desirable in disposition of this application, the Examiner is respectfully requested to call the undersigned attorney at (603) 668-6560.

In the event there are any fee deficiencies, please charge them (or credit any overpayment) to our Deposit Account No. 50-2121.

Respectfully submitted,

Scott R. Faber
Attorney for Applicant
Reg. No. 48,380

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